CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A tertiary content addressable memory (CAM) cell, comprising:

a first storage element having a first capacitor controllably coupled via a first switch to a first bit line;

a second storage element having a second capacitor controllably coupled via a second switch to a second bit line;

a third storage element having a third capacitor controllably coupled via a third switch to a third bit line;

wherein said first, second, and third storage elements are coupled to a control circuit which, in response to one of said storage elements being set to a first logical state, sets each of the other storage elements to a second logical state.

2. The tertiary CAM cell of claim 1, wherein said first, second, and third switches are transistors.

3. The tertiary CAM cell of claim 1, wherein said control circuit further comprises,

a first pair of controllable discharge devices, coupled in parallel between a ground potential and the first capacitor;

a second pair of controllable discharge devices, coupled in parallel between the ground potential and the second capacitor; and

a third pair of controllable discharge devices, coupled in parallel between the ground potential and the third capacitor;

wherein

said first pair of controllable discharge devices are arranged to set said first capacitor to correspond to the second logical state if either the second or third capacitors are set to store a charge associated with the first logical state;

said second pair of controllable discharge devices are arranged to set said second capacitor to correspond to the second logical state if either the first or third capacitors are set to store a charge associated with the first logical state; and

said third pair of controllable discharge devices are arranged to set said third capacitor to correspond to the second logical state if either the first or second capacitors are set to store a charge associated with the first logical state.

4. The CAM cell of claim 3, wherein said controllable discharge devices are transistors having a first source/drain terminal coupled to a first terminal of one of said storage capacitors and a second source/drain terminal coupled to the ground potential.

5. A tertiary content addressable memory (CAM) cell, comprising:

a first, second, and third bit lines;

a select line;

a first, second, and third access transistors, wherein each of said first, second, and third access transistors include a gate coupled to said select line and a first terminal coupled to a respective one of said first, second, and third bit lines, and a second terminal coupled to a respective one of said first, second, and third storage units;

wherein each of said first, second, and third storage units include,

a storage capacitor coupled between a respective second terminal of a respective first, second, and third transistors and a ground potential;

a first discharge transistor having a gate coupled to the second terminal of a first of the two other storage units, a first source/drain terminal coupled to the storage capacitor, and a second source/drain terminal coupled to the ground potential;

a second discharge transistor having a gate coupled to the second terminal of a second of the two other storage units, a first source/drain terminal coupled to the storage capacitor, and a second source/drain terminal coupled to the ground potential.

6. A tertiary content addressable memory (CAM) device, comprising:

a priority encoder;

match detection circuit, coupled to said priority encoder; and

a CAM array, coupled to said match detection circuit, and including a plurality of CAM cells, further comprising,

a first storage element having a first capacitor controllably coupled via a first switch to a first bit line;

a second storage element having a second capacitor controllably coupled via a second switch to a second bit line;

a third storage element having a third capacitor controllably coupled via a third switch to a third bit line;

wherein said first, second, and third storage elements are coupled to a control circuit which, in response to one of said storage elements being set to a first logical state, sets each of the other storage elements to a second logical state.

7. The device of claim 6, wherein said first, second, and third switches are transistors.

8. The device of claim 6, wherein said control circuit further comprises,

a first pair of controllable discharge devices, coupled in parallel between a ground potential and the first capacitor;

a second pair of controllable discharge devices, coupled in parallel between the ground potential and the second capacitor; and

a third pair of controllable discharge devices, coupled in parallel between the ground potential and the third capacitor;

wherein

said first pair of controllable discharge devices are arranged to set said first capacitor to correspond to the second logical state if either the second or third capacitors are set to store a charge associated with the first logical state;

said second pair of controllable discharge devices are arranged to set said second capacitor to correspond to the second logical state if either the first or third capacitors are set to store a charge associated with the first logical state; and

said third pair of controllable discharge devices are arranged to set said third capacitor to correspond to the second logical state if either the first or second capacitors are set to store a charge associated with the first logical state.

9. The CAM cell of claim 8, wherein said controllable discharge devices are transistors having a first source/drain terminal coupled to a first terminal of one of said storage capacitors and a second source/drain terminal coupled to the ground potential.

10. A network device, comprising:

a first network interface;

a second network interface;

a control logic for deciding whether forward packet received on the first network interface to the second network interface, said control logic including a plurality of tertiary CAM cells, said CAM cells further comprising,

a first storage element having a first capacitor controllably coupled via a first switch to a first bit line;

a second storage element having a second capacitor controllably coupled via a second switch to a second bit line;

a third storage element having a third capacitor controllably coupled via a third switch to a third bit line;

wherein said first, second, and third storage elements are coupled to a control circuit which, in response to one of said storage elements being set to a first logical state, sets each of the other storage elements to a second logical state.

11. The network device of claim 10, wherein said first, second, and third switches are transistors.

12. The network device of claim 10, wherein said control circuit further comprises,

a first pair of controllable discharge devices, coupled in parallel between a ground potential and the first capacitor;

a second pair of controllable discharge devices, coupled in parallel between the ground potential and the second capacitor; and

a third pair of controllable discharge devices, coupled in parallel between the ground potential and the third capacitor;

wherein

said first pair of controllable discharge devices are arranged to set said first capacitor to correspond to the second logical state if either the second or third capacitors are set to store a charge associated with the first logical state;

said second pair of controllable discharge devices are arranged to set said second capacitor to correspond to the second logical state if either the first or third capacitors are set to store a charge associated with the first logical state; and

said third pair of controllable discharge devices are arranged to set said third capacitor to correspond to the second logical state if either the first or second capacitors are set to store a charge associated with the first logical state.

13. The network device of claim 12, wherein said controllable discharge devices are transistors having a first source/drain terminal coupled to a first terminal of one of said storage capacitors and a second source/drain terminal coupled to the ground potential.

14. A method for operating a tertiary content addressable memory (CAM) cell, comprising:

setting a first of three binary storage elements to a first binary state to indicate a first tertiary state of said CAM cell,

wherein in response to said first binary storage element being set to a first binary state, said second and third binary storage elements are each set to a second binary state.

15. The method of claim 14, further comprising,

setting the second of three binary storage elements to a first binary state to indicate a second tertiary state of said CAM cell,

wherein in response to said second binary storage element being set to a first binary state, said first and third binary storage elements are each set to a second binary state.

16. The method of claim 15, further comprising,

setting the third of three binary storage elements to a first binary state to indicate a third tertiary state of said CAM cell,

wherein in response to said third binary storage element being set to a first binary state, said first and second binary storage elements are each set to a second binary state.

17. The method of claim 16, wherein said first, second, and third tertiary states are members of a set consisting of the following elements,

a binary "0";

a binary "1"; and

a "don't care" state.

18. The method of claim 14, further comprising:

reading the state of said first binary storage element, said reading further comprising the steps of,

precharging a first bit line controllably coupled to said first storage element to a predetermined level;

coupling said first bit line to said first binary storage element; and

coupling, sensing a change in potential of said first bit line;

wherein said reading does not change the state of said first storage element.

19. The method of claim 15, further comprising:

reading the state of said second binary storage element, said reading further comprising the steps of,

precharging a second bit line controllably coupled to said second storage element to a predetermined level;

coupling said second bit line to said second binary storage element; and

sensing a change in potential of said second bit line;

wherein said reading does not change the state of said second storage element.

20. The method of claim 16, further comprising:

reading the state of said third binary storage element, said reading further comprising the steps of,

precharging a third bit line controllably coupled to said third storage element to a predetermined level;

coupling said third bit line to said third binary storage element; and

after said coupling, sensing a change in potential of said third bit line;

wherein said reading does not change the state of said third storage element.